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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/863,888 | 05/22/2001 | Anthony William Jorgenson | 5957-41000 | 9420 |

35690 7590 01/10/2007

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| EXAMINER | |
|---|---|
| JUNTIMA, NITTAYA | |
| ART UNIT | PAPER NUMBER |
| 2616 | |

| SHORTENED STATUTORY PERIOD OF RESPONSE | MAIL DATE | DELIVERY MODE |
|---|---|---|
| 3 MONTHS | 01/10/2007 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/863,888 | JORGENSON ET AL. | |
| | Examiner | Art Unit | |
| | Nittaya Juntima | 2616 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *01 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1,9-12,22-24,54,56 and 71-87* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,9-12,22,54,56,71-82 and 85* is/are rejected.

7)☒ Claim(s) *23-24,83-84,86-87* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 May 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

1. This action is in response to the amendment filed on 12/1/2006.

2. Claims 2-8, 13-21, 25-53, 55, and 57-70 were cancelled.

3. The indicated allowable subject matter in the previous Office action is withdrawn in view of the newly discovered reference(s). Rejections based on the newly cited reference(s) follow.

4. Accordingly, claims 54 and 56 are presently rejected under 35 U.S.C. 102(b).

5. Claims 1, 12, and 22 are rejected under 35 U.S.C. 102(e)

6. Claims 9-11, 71-82, and 85 are presently rejected under 35 U.S.C. 103(a).

7. Claims 23-24, 83-84, and 86-87 are currently objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

### *Claim Rejections - 35 USC § 102*

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 54 and 56 are rejected under 35 U.S.C. 102(b) as being anticipated by Upp (US 5,040,170).

Regarding claim 54, as shown in Figs. 1 and 2b, Upp teaches an apparatus for providing data transport through a data network, comprising:

A clock recovery unit (a clock recovery function is not claimed, therefore, a clock recovery unit reads on a SONET line interface 100, Fig. 1 which provides frame clock) configured to receive an encoded data (data is encoded in a SONET STS-24 signal). See col. 6, lines 16-24.

A data translation unit (8:1 demux control 273, Fig. 2b demultiplexes the incoming STS-24 signal into two STS-12 signals) coupled to said clock recovery unit, configured to translate said received data to a predetermined data (col. 9, lines 21-32).

An inverse multiplexer (4:1 controller 278, Fig. 2b demultiplexes two STS-12 signals into two sets of four STS-3 signals) coupled to said data translation unit, configured to inverse multiplex said translated predetermined data.

A modem (modulation function is not claimed, therefore, a modem reads on the STS-3 output blocks 290 that receive the STS-3 signals and output them, col. 9, lines 45-48) coupled to said inverse multiplexer configured to receive said inverse multiplexed translated predetermined data for transmission, wherein said inverse multiplexed translated predetermined data includes a plurality of STS-3 signals.

Regarding claim 56, Upp teaches that said plurality of STS-3 signals includes eight STS-3 signals for transmission (col. 9, lines 28-31 and 45-48).

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an

international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

11. Claims 1, 12, and 22 are rejected under 35 U.S.C. 102(e) as being anticipated by Ouellet (US 6,854,031 B1).

Regarding claims 1 and 12, Ouellet teaches an apparatus (22-E in Fig. 2) for providing data transport through a data network, comprising:

A clock recovery unit (SerDes 34-E in Fig. 3) configured to receive an encoded data including 8B/10B encoded data (col. 6, lines 27-29, 25-27, 44-52).

A data translation unit (FIFO_1 80_1 in Fig. 10 decodes the 10-bit data into 8-bit data) coupled to said clock recovery unit, configured to translate said received data to a predetermined data (col. 11, lines 24-25).

An inverse multiplexer (DEMUX 84 in Fig. 10) coupled to said data translation unit, configured to inverse multiplex said translated predetermined data (col. 11, lines 25-26).

Wherein said clock recovery unit (SerDes 34-E in Fig. 3) is further configured to recover a clock signal from said received encoded data (col. 5, lines 52-56), wherein said clock signal (125 MHz) has a rate one tenth of said data rate (1.25Gb/s) (col. 5, lines 52-56, col. 10, lines 60-64, and Fig. 10).

Regarding claim 22, Oullet teaches a modem coupled to said inverse multiplexer configured to receive said inverse multiplexed translated predetermined data for transmission (modulation function is not claimed, therefore, a modem reads on the Rx FIFO 88 that receives the signal from DEMUX 84 for further transmission, col. 11, lines 24-31).

***Claim Rejections - 35 USC § 103***

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ouellet (US 6,854,031 B1) in view of Moshe (US 6,914,941 B1).

Regarding claims 9-11, the teaching of Ouellet does not teach the step of synchronizing said inverse multiplexed predetermined data to a predetermined clock signal including a phase locked loop clock signal.

However, as shown in Fig. 3, Moshe teaches an analogous art where an inverse multiplexing (102) includes synchronizing an inverse multiplexed predetermined data to a predetermined clock signal which includes a phase locked loop clock signal (112), col. 6, lines 5-13 and 27-32.

Given the teaching of Moshe, it would have been obvious to one skilled in the art at the time of the invention to further modify the teaching of Ouellet to include the step of synchronizing said inverse multiplexed predetermined data to a predetermined clock signal including a phase locked loop clock signal. The suggestion/motivation to do so would have been to keep the data rate, i.e. data rate going into the DEMUX 84 in Fig. 10 of Ouellet, constant as suggested by Moshe (col. 6, lines 8-11).

14. Claims 71-73 are rejected under 35 U.S.C. 103(a) as being unpatentable over Azizoglu (US 6,430,201 B1) in view of Henson (US 6,158,014).

As shown in Fig. 2, Azizoglu teaches receiving an encoded data, wherein said encoded data includes 8B/10B data (20-1 receives GbE signal encoded with 8B/10B, col. 4, lines 38-44).

Mapping said received data to a predetermined data (data from GbE signal is decoded by 8b/10 codec 22-1 into an 8 bits parallel stream, col. 4, lines 42-49).

Inverse multiplexing said mapped predetermined data (a deinterleaver 64, Fig. 4 at the receiving side receives and demultiplexes the incoming data containing the 8 bits parallel stream transmitted from the transmitting side via a WDM combiner 16 in Fig. 1 and put the 8 bits parallel stream into an appropriate 8b/10b codec, col. 6, lines 4-14, see also Figs. 1 and 3).

However, Azizoglu fails to teach that determining a data rate of said received encoded data.

As shown in Fig. 1, Henson teaches determining a data rate of received 8B/10B encoded data in Gigabit Ethernet network (the pattern recognition logic 120 determines the data rate of a 8B/10B serial stream, col. 3, lines 41-46, 62-col. 4, lines 1-14).

Therefore, it would have been obvious to one skilled in the art at the time of the invention to modify the teaching of Azizoglu to include the step of determining a data rate of said received encoded data as claimed. The suggestion/motivation to do so would have been to enable the system to positively identify the transmission data rate of the received data and operate at more than one data rate as suggested by Henson (col. 3, lines 5-24 and 40-45).

Regarding claim 72, Azizoglu teaches that the encoded data includes a Gigabit Ethernet data (Fig. 2).

Regarding claim 73, Azizoglu does not teach recovering a clock signal from said received encoded data. However, Henson teaches recovering a clock signal from said received encoded

data (col. 4, lines 12-17 and 28-32). Therefore, it would have been obvious to one skilled in the art at the time of the invention to modify the teaching of Azizoglu to include the step of recovering a clock signal from said received encoded data as recited in the claim. The suggestion/motivation to do so would have been to enable the system to match the clock speed of a deserializer (e.g. 20-1 in Fig. 2 of Azizoglu) to that of the data rate of the serial bitstream (Henson, col. 4, lines 30-32).

15. Claims 75-77 and are rejected under 35 U.S.C. 103(a) as being unpatentable over Azizoglu (US 6,430,201 B1) in view of Henson (US 6,158,014), and further in view of Moshe (US 6,914,941 B1).

Regarding claims 75-77, the combined teaching of Azizoglu and Henson does not teach the step of synchronizing said inverse multiplexed predetermined data to a predetermined clock signal including a phase locked loop clock signal.

However, as shown in Fig. 3, Moshe teaches an analogous art where an inverse multiplexing (102) includes synchronizing an inverse multiplexed predetermined data to a predetermined clock signal which includes a phase locked loop clock signal (112), col. 6, lines 5-13 and 27-32.

Given the teaching of Moshe, it would have been obvious to one skilled in the art at the time of the invention to further modify the combined teaching of Azizoglu and Henson to include the step of synchronizing said inverse multiplexed predetermined data to a predetermined clock signal including a phase locked loop clock signal. The suggestion/motivation to do so would have been to keep the input data rate, i.e. bit rate of the data, which contains the 8 bits

parallel stream from the transmitting side, going into the Deinterleaver 64 in Fig. 4 of Azizoglu, constant through the transmission path as suggested by Moshe (col. 6, lines 8-11).

16. Claims 71-74, 78-82, and 85 and are rejected under 35 U.S.C. 103(a) as being unpatentable over Ouellet (US 6,854,031 B1) in view of Henson (US 6,158,014).

Regarding claims 71 and 78, Ouellet teaches an apparatus (22-E in Fig. 2) for providing data transport through a data network, comprising:

A clock recovery unit (SerDes 34-E in Fig. 3) configured to receive an encoded data including 8B/10B encoded data (col. 6, lines 27-29, 25-27, 44-52).

A data translation unit (FIFO_1 80_1 in Fig. 10 decodes the 10-bit data into 8-bit data) coupled to said clock recovery unit, configured to translate said received data to a predetermined data (col. 11, lines 24-25).

An inverse multiplexer (DEMUX 84 in Fig. 10) coupled to said data translation unit, configured to inverse multiplex said translated predetermined data (col. 11, lines 25-26).

However, Oullet does not teach that the clock recovery unit is further configured to detect a data rate of the received encoded data.

As shown in Fig. 1, Henson teaches determining a data rate of received 8B/10B encoded data in Gigabit Ethernet network using the pattern recognition logic 120, col. 3, lines 41-46, 62-col. 4, lines 1-14.

Since Oullet teaches that the incoming line rates can be OC-48 or OC-12 (col. 11, lines 9-10 and 24-25), it would have been obvious to one skilled in the art at the time of the invention to modify the teaching of Oullet to apply the concept of detecting the data rate such that the clock

recovery unit would be able to detect a data rate of the received encoded data as claimed, i.e. by integrating the functions of the pattern recognition of Henson into the SerDes of Oullet. The suggestion/motivation to do so would have been to enable the system to positively identify the transmission data rate of the received data and operate at more than one data rate as suggested by Henson (col. 3, lines 5-24 and 40-45).

Regarding claims 72 and 79, Oullet teaches that the encoded data includes a Fiber channel data (OC-12, col. 6, lines 25-27 and col. 11, lines 24-27).

Regarding claims 73 and 80, Oullet teaches that said clock recovery unit (SerDes 34-E in Fig. 3) configured to recover a clock signal from said received encoded data (col. 5, lines 52-56).

Regarding claims 74 and 81, Oullet teaches that said clock signal (125 MHz) has a rate one tenth of said data rate (1.25Gb/s) (col. 5, lines 52-56, col. 10, lines 60-64, and Fig. 10).

Regarding claim 82, Oullet teaches a modem coupled to said inverse multiplexer configured to receive said inverse multiplexed translated predetermined data for transmission (modulation function is not claimed, therefore, a modem reads on the Rx FIFO 88 that receives the signal from DEMUX 84 for further transmission, col. 11, lines 24-31).

Regarding claim 85, Ouellet teaches an apparatus (22-E in Fig. 2) for providing data transport through a data network, comprising:

A clock recovery unit (SerDes 34-E in Fig. 3) configured to receive an encoded data including 8B/10B encoded data (col. 6, lines 27-29, 25-27, 44-52).

A data translation unit (FIFO_1 80_1 in Fig. 10 decodes the 10-bit data into 8-bit data) coupled to said clock recovery unit, configured to translate said received data to a predetermined data (col. 11, lines 24-25).

An inverse multiplexer (DEMUX 84 in Fig. 10) coupled to said data translation unit, configured to inverse multiplex said translated predetermined data (col. 11, lines 25-26).

A modem coupled to said inverse multiplexer configured to receive said inverse multiplexed translated predetermined data for transmission (modulation function is not claimed, therefore, a modem reads on the Rx FIFO 88 that receives the signal from DEMUX 84 for further transmission, col. 11, lines 24-31).

However, Oullet does not teach that the clock recovery unit is further configured to detect a data rate of the received encoded data.

As shown in Fig. 1, Henson teaches determining a data rate of received 8B/10B encoded data in Gigabit Ethernet network using the pattern recognition logic 120, col. 3, lines 41-46, 62-col. 4, lines 1-14.

Since Oullet teaches that the incoming line rates can be OC-48 or OC-12 (col. 11, lines 9-10 and 24-25), it would have been obvious to one skilled in the art at the time of the invention to modify the teaching of Oullet to apply the concept of detecting the data rate such that the clock recovery unit would be able to detect a data rate of the received encoded data as claimed, i.e. by integrating the functions of the pattern recognition of Henson into the SerDes of Oullet. The suggestion/motivation to do so would have been to enable the system to positively identify the transmission data rate of the received data and operate at more than one data rate as suggested by Henson (col. 3, lines 5-24 and 40-45).

17. Claims 75-77 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ouellet (US

6,854,031 B1) in view of Henson (US 6,158,014), and further in view of Moshe (US 6,914,941 B1).

Regarding claims 75-77, the combined teaching of Ouellet and Henson does not teach the step of synchronizing said inverse multiplexed predetermined data to a predetermined clock signal including a phase locked loop clock signal.

However, as shown in Fig. 3, Moshe teaches an analogous art where an inverse multiplexing (102) includes synchronizing an inverse multiplexed predetermined data to a predetermined clock signal which includes a phase locked loop clock signal (112), col. 6, lines 5-13 and 27-32.

Given the teaching of Moshe, it would have been obvious to one skilled in the art at the time of the invention to further modify the combined teaching of Ouellet and Henson to include the step of synchronizing said inverse multiplexed predetermined data to a predetermined clock signal including a phase locked loop clock signal. The suggestion/motivation to do so would have been to keep the data rate, i.e. data rate going into the DEMUX 84 in Fig. 10 of Ouellet, constant as suggested by Moshe (col. 6, lines 8-11).

***Conclusion***

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nittaya Juntima whose telephone number is 571-272-3120. The examiner can normally be reached on Monday through Friday, 8:00 A.M - 5:00 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on 571-272-3155. The fax phone number for the

organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Nittaya Juntima
January 5, 2007
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